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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,390	10/30/2001	Jae-Yong Jeong	4591-220	5348

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ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/003,390	JEONG ET AL.
	Examiner	Art Unit
	Christine T. Tu	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 21-30* is/are rejected.

7)☒ Claim(s) *19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. Claims 1-7, 10-11, 13 and 21-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

At lines 3-6, it is not clear when and how the fail memory cells are determined before the fail bit counter can count them. In other words, a step of determining fail bits should be performed first in order for the fail bit counter to count them.

Claims 4 and 5:

Claim 4 or claim 5 should be canceled due to duplicate claims 4 and 5 because they contain same limitations.

Claim 7:

At line 2, insert a comma "," after the term "test operation".

At line 2, insert a word "data" before the word "bits".

Claim 10:

The phrase "the clock signals are read-out enable signals" is not logic. It is not clear how clock signals (CLK) can be read (out) enable signals (RE). In other words, clock signals (CLK) should control timing or synchronization and read enable signals (RE) should enable the read function.

Claim 11:

At line 2, the verb "initialized" should be replaced with –incremented--- due to the fact that the fail bit counter and latch circuit should be incremented a count number. In other words, the fail bit counter and latch circuit is NOT set to "zero" (as being recited in the claimed).

Claim 13:

The term "the clock signals" at line 3 lacks antecedent basis.

Claim 21:

At line 7, the term "the compared outputted expected data" lacks antecedent basis. It is not clear where is the compared outputted expected data coming from.

At line 7, the term "a register" should be replaced with –the expected data buffer—if the term refers to the previously recited buffer (as claimed at line 4). In other words, consistency of a term should be used throughout the claims.

At lines 6-7, it is not clear when and how the inputted expected data is determined to be not corresponding to the compared outputted expected data in a register. What is the purpose for registering such failure occasions of non-correspondence of the inputted expected data and the compared outputted expected data.

Claim 27:

At line 8, how is a fail code determined? And how is the fail code different from the counted number?

At lines 9-10, it is not clear when and how the column address is being incremented due to the recited phrase "after incrementing the column address" at line 10. In other words, a step of incrementing the column address should be recited in the claim.

Claims 2-3, 6, and 22-26, 28-30:

These claims are rejected because they depend on claims 1, 21 and 27 and contain the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor

and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-18 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al. (6,243,840 and Raad hereinafter) in view of Hill et al. (6,141,779 and Hill hereinafter).

Claims 1 and 2:

Raad disclosed the invention substantially as claimed. Raad shows (figure 1) a memory device (10) comprising a memory array (11A) having plurality of memory cells and a data output register (28) for outputting the read data from the memory array (11A) (figure 1, column 3 line 1 – column 4 line 9).

Raad also shows (figures 1 & 3) that a test mode circuit (36) comprises a data compare circuit (38) for comparing data from array (37) to a predetermined 32-bit data pattern from a data background circuit (40) (column 5 line 58-column 6 line 4).

Raad does not teach the fail bit counter. Hill, however, teaches a combination of a sticky compare register (142) and a counter (144). The sticky compare register (142) has plurality of bits each for storing a "1" in corresponding to a failed cell (104) in a column of a memory array (102). The counter (144) then counts the number of bits of the sticky compare register (142) that contains a "1" (figure 3, column 5 line 54-column 6 line 3).

It would have been obvious to one skilled in the art at the time the invention was made to connect the combination of the sticky compare register (142) and the counter (144) (as taught by Hill) to Raad's data compare circuit (38) for counting the number of bad bits in the memory. One having ordinary skill in the art would have be motivated to so because (1) Hill teaches the sticky compare register (142) is connected to the outputs of a comparator (132) having XOR gates [figure 3], and (2) Raad teaches that the comparator (38) comprising logic gate structure which can be implemented by any designs well known to the art (figure 3, column 5 lines 62-64).

Claim 3:

Hill teaches that the content of the counter (144) contains the endoded RAM redundancy map value (column 6 line 3-7).

Claims 4 and 5:

Raad teaches that the test mode circuit (36) is located between the memory array (11A) and the data output register (28) (figure 1).

Claim 6:

Raad's data compare circuit (38) compares data from array (37) to a predetermined 32-bit data pattern from a data background circuit (40) (figure 3, column 5 line 58-column 6 line 4).

Claim 7:

Raad teaches the predetermined data pattern that contained in the data background circuit (40) is also written to the memory device (10) (column 6 lines 5-7).

Claim 8 and 11:

Raad disclosed the invention substantially as claimed. Raad shows (figures 1 & 3) a memory device (10) comprising a memory array (11A) having plurality of memory cells arranged in rows and columns, a row latch and decode circuit (18A) activates a selected row of memory cells in responsive to a row address, a combination of a column latch and decode circuit (20) and I/O interface circuit (26A) gates data from memory cells in responsive to a column address, a background circuit (40) in a test mode circuit (36), for storing a predetermined 32-bit data pattern (figures 1 & 3, column 3 line 1 – column 4 line 9, column 5 lines 60-63).

Raad also shows (figures 1 & 3) that a test mode circuit (36) comprises a data compare circuit (38) for comparing data from array (37) to a predetermined 32-bit data pattern from a data background circuit (40) in response to a STE signal wherein the data compare circuit (38) produce a pass/fail signal based on the comparison result (column 5 line 58-column 6 line 21).

Raad does not teach the fail bit counter. Hill, however, teaches a combination of a sticky compare register (142) and a counter (144). The sticky compare register (142) has plurality of bits each for storing a "1" in corresponding to a failed cell (104) in a column of a memory array (102). The counter (144), being initialized to zero, counts the number of bits of the sticky compare register (142) that contains a "1" and contains the encoded RAM redundancy map value (figure 3, column 5 line 54-column 6 line 7).

It would have been obvious to one skilled in the art at the time the invention was made to connect the combination of the sticky compare register (142) and the counter (144) (as taught by Hill) to Raad's data compare circuit (38) for counting the number of bad bits in the memory. One having ordinary skill in the art would have be motivated to so because (1) Hill teaches the sticky compare register (142) is connected to the outputs of a comparator (132) having XOR gates [figure 3], and (2) Raad teaches that the comparator (38) comprising logic gate structure which can be implemented by any designs well known to the art (figure 3, column 5 lines 62-64).

Claims 9 & 10:

Raad's comparator (38) is enabled by a signal STE at the time referenced to the system clock signal CLK (column 5 line 66-column 6 line 4).

Claims 12 & 13:

Raad teaches that a data output register (28), which connected to the I/O pins (DQ0-DQ31), is disabled and prevented data to be outputted in response to a failed comparison of the comparator (38) (figure 1, column 6 lines 17-21).

Claims 14-15:

Raad teaches the combination of the I/O interface circuit (26A) and the data output register (28) such that the I/O interface circuit (26A) loads data from the memory array (11A) into the test mode circuit (36) and data output register

(28) via an internal data output bus (37). The data output register (28) is connected to I/O pins (DQ0-DQ31). The test mode circuit (36) has a comparator (38) for comparing data from the internal data output bus to a predetermined data pattern from the data background circuit (40). If a data mismatch occurs, the data compare circuit sends a failed comparison (P/F) signal to prevent data to be outputted from the data output register (28) (figures 1 & 3, column 5 line 55-column 6 line 27).

Claims 16-18:

Hill teaches that the comparator (132) including plurality of XOR gates each of which outputs a "1" if a mismatch is detected. The output "1" is then load into the sticky compare register (142). Each of the "1" will be right shifted from the sticky compare register (142) in responsive to the shift clock (figure 3, column 54-62, column 6 lines 28-35).

Claims 21, 22, and 24-25:

Claims (21 & 24), 22 and 25 are rejected for reasons similar to those set forth against claims (1 & 2), 7 and 3, respectively.

Claim 23:

Raad teaches a signal STE enables the comparison in the comparator (38) (column 5 line 66-column 6 line 4).

Claim 26:

Hill's counter (144) is initialized (column 5 line 57-68).

5. Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raad et al. (6,243,840 and Raad hereinafter) in view of Hill et al. (6,141,779 and Hill hereinafter) and Beffa et al. (6,032,264 and Beffa hereinafter).

Claim 27:

Raad disclosed the invention substantially as claimed. Raad shows (figure 1) within a memory device (10), the feature of accessing the memory cells in a memory array (11A) and the feature of reading data from the accessed memory cells corresponding to the address by sending the requisite control signals to the column-address latch and decode circuit (20) and an I/O interface circuit (26A). Raad also teaches that the data read (37) is then compared by a comparator (38) to a pattern of the data background circuit (40) (figures 1 & 3, column 6 lines 52-65).

Raad does not teach the feature of counting the number of unmatched data bits nor the feature of storing a fail code determined according to the counted number. Hill, however, teaches a combination of a sticky compare register (142) and a counter (144). The sticky compare register (142) has plurality of bits each for storing a "1" in corresponding to a failed cell (104) in a column of a memory array (102). The counter (144) then counts the number of bits of the sticky compare register (142) that contains a "1". The contents of the

counter (144) contain the encoded RAM redundancy map value which may be loaded into nonvolatile storage (146) (figure 3, column 5 line 54-column 6 line 7).

It would have been obvious to one skilled in the art at the time the invention was made to connect the combination of the sticky compare register (142) and the counter (144) (as taught by Hill) to Raad's data compare circuit (38) for counting the number of bad bits in Raad's memory. One having ordinary skill in the art would have be motivated to so because (1) Hill teaches the sticky compare register (142) is connected to the outputs of a comparator (132) having XOR gates [figure 3], and (2) Raad teaches that the comparator (38) comprising logic gate structure which can be implemented by any designs well known to the art (figure 3, column 5 lines 62-64).

Raad does not explicitly teach the feature of performing repeatedly the selecting, determining, counting and storing steps until a maximum of column address is reach. Beffa, however, teaches under the control of a control circuitry (222), a semiconductor (200) performs the feature of repeatedly accessing memory cell addressed by an incremented content of a column counter (606), the feature of determining repeatedly whether the memory cell is defected (608), if there is a defect, incrementing the number of cell failures until maximum of column address is reach (612, 610) (figures 2 and 6A, column 6 lines 25-61, column 5 lines 25-42).

It would have been obvious to one skilled in the art at the time the invention was made to use additional controls from Beffa's control circuitry to carry out the repeatedly accessing, determining and incrementing features for

memory testing in Raad's memory device (10). One having ordinary skill in the art would have be motivated to so because Raad suggests that each memory cell or bit of the memory device must be tested in order to provide a reliable memory device (column 1 lines 13-23).

Claim 28:

The comparator (38) is enabled in responsive to a STE signal (figure 3, column 5 line 67-column 6 line 4).

Claim 29:

Hill teaches that the contents of the sticky compare register (142) are encoded and stored into a nonvolatile storage (146) (column 5 lines 63-65).

Claim 30:

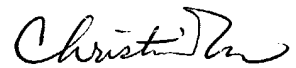
Beffa teaches that the feature of setting the number of failures to zero (618) after all memory cells in the present row has been tested (figures 6A & 6B).

6. Claims 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (703)305-9689. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703)305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christine T. Tu
Primary Examiner
Art Unit 2133

August 5, 2004